

The heteroepitaxy of Ge on Si: A comparison of chemical vapor and vacuum deposited layers

M. Mäenpää,^{a)} T. F. Kuech, and M-A. Nicolet
California Institute of Technology, Pasadena, California 91125

S. S. Lau
University of California at San Diego, La Jolla, California 92093

D. K. Sadana
Lawrence Berkeley Laboratory, Berkeley, California 94720

(Received 20 August 1981; accepted for publication 6 October 1981)

Epitaxial growth of Ge on Si has been investigated by two techniques: vacuum deposition and chemical vapor deposition (CVD). Vacuum-deposited Ge layers (physical vapor deposition, PVD) on heated Si substrates ($\leq 500^\circ\text{C}$) have smooth surface morphologies with a surface crystalline quality which improves with Ge layer thickness. Layers prepared by the CVD technique at $500\text{--}600^\circ\text{C}$ are comparable with the PVD prepared layers. Main defects in both PVD and CVD layers are dislocations initiating at the Ge/Si interface. Chemical vapor-deposited Ge layers grown at a substrate temperature of $700\text{--}800^\circ\text{C}$ exhibit poor crystalline quality and often are polycrystalline. Chemical vapor-deposited layers grown at a substrate temperature of 900°C , again are good quality epitaxial layers. In this case, in addition to dislocations, stacking faults are present. All the studied layers are highly conductive and *p*-type. The conduction and valence band discontinuities determined from electrical measurements are $0.05 \pm 0.04\text{ eV}$ and $0.39 \pm 0.04\text{ eV}$, respectively.

PACS numbers: 73.40.Lq, 68.55.+b, 81.15.Ef, 81.15.Gh

I. INTRODUCTION

The possibility of integrating GaAs and Si devices in a single monolithic structure has motivated the recent increased interest in the heteroepitaxial growth of both Ge^{1-8} and $\text{Ge}_x\text{Si}_{1-x}^{1,2,9}$ alloys on Si. Since GaAs can be easily grown on Ge, a high quality epitaxial Ge layer on Si has been shown to serve as a suitable substrate for the subsequent growth of GaAs^{3,4} and possibly other layers (e.g., $\text{Ga}_x\text{Al}_{1-x}\text{As}$). This would allow for the possibility of integration of GaAs optoelectronic devices with Si-based electronic devices. Interest in this heterojunction system is also due to the chemical simplicity of the Ge-Si heterojunction system. Since Ge and Si form a complete solid solution, Ge-Si heterojunctions are considered one of the simplest examples of heterojunctions crystal growth and behavior, a fact which motivated their early study.¹⁰⁻¹⁴ A complicating factor in this heterojunction system, however, is a large mismatch in both lattice parameter ($\sim 4\%$) and thermal expansion coefficient ($\sim 50\%$) between Ge and Si.

The majority of recent studies have utilized vacuum deposition of Ge in fabrication of the Ge-Si heterojunction. Initial recent attempts formed the heterojunction by vacuum depositing a layer of amorphous Ge on $\langle 100 \rangle$ Si substrate. The amorphous Ge layers were then heated by pulsed laser and/or electron beam irradiation.^{1,2} This annealing step leads to the melting of the Ge layer and dissolution of Si from the substrate surface. A $\text{Ge}_x\text{Si}_{1-x}$ alloy solidifies upon cooling. The presence of a fast moving liquid-solid interface in this two-component system leads to cellular structures and results in poor epitaxial quality of the Ge layer. The solid-phase growth at $\sim 500\text{--}700^\circ\text{C}$ of vacuum-deposited amor-

phous Ge layers on chemically cleaned Si substrates yielded epitaxial Ge layers without cellular structures. The crystalline quality of these layers was still relatively poor.^{3,5} The quality of these epitaxial layers can be improved by an ion implantation step followed by annealing in vacuum. This implantation step promotes layer-by-layer growth in the surface region of the Ge layer amorphized by ion irradiation and leads to improved crystalline quality.^{3,5} Early studies of this heteroepitaxial system demonstrated that heating the Si substrate to $500\text{--}700^\circ\text{C}$ during the vacuum deposition of Ge results in epitaxial growth.¹¹⁻¹³ This has been clearly shown in a recent study by Tsaui *et al.*⁴ The hot substrate deposition procedure eliminates the need for a post-deposition annealing step. The crystalline perfection of these epitaxial Ge layers is better than those obtained by solid-phase growth^{3,5} and similar to those obtained by the implantation-annealing technique.^{3,5}

All attempts to produce Ge/Si heterostructures mentioned above utilized vacuum deposition of Ge on Si substrates. The Ge layers produced in these studies exhibited a marked variation in the growth morphology and crystalline quality. This variation is attributed to contamination present at the Ge-Si interface, determined primarily by the initial condition of the Si substrate surface and the details of the deposition procedure. Carbon and oxygen have been found to influence both growth morphology and growth rate in both the epitaxy of Si on Si¹⁵ and Ge on Si.¹²

It has recently been shown that a simple chemical vapor deposition (CVD) technique utilizing the decomposition of GeH_4 on a Si substrate produces epitaxial layers with good crystalline quality.^{6,8} While CVD has long provided a fast, clean, and inexpensive method of growing high-purity semiconductor materials, little work has been done on the application of CVD techniques to the Ge-Si system.¹⁰

^{a)}Permanent address: Semiconductor Laboratory, Technical Research Centre of Finland, Otakaari 5A, SF-02150 Espoo 15, Finland.

The study presented here was undertaken to investigate and contrast the growth characteristics of epitaxial Ge layers deposited on Si produced by these two methods: namely, chemical vapor deposition (CVD) and physical vapor deposition (PVD) (i.e., vacuum deposition onto heated substrates). Electrical behavior of these Ge layers and the resulting heterojunctions formed by PVD and CVD are also presented. Vacuum-deposited Ge layers were grown in this study under ultra-high vacuum (UHV) ion-pumped conditions, eliminating the carbon impurity source found in oil diffusion pumped systems. Since the initial Si substrate preparation was the same in both the PVD and CVD growth systems, PVD Ge layers in this study would serve as a suitable controlled basis of comparison for the CVD grown layers.

II. EXPERIMENTAL

A. Silicon substrate preparation

Substrates of both *p*- and *n*-(<100) Si (1–10 Ω cm) were initially prepared by thermally oxidizing the Si wafer at 1050 °C in dry O₂, producing an oxide layer ≥ 2000 Å in thickness. Immediately prior to the introduction of the substrate into either of the growth systems (vacuum chamber or CVD growth reactor), the oxide was removed by etching in a concentrated HF solution (1 : 1, HF : H₂O). This procedure has been found to produce a clean reproducible Si surface free of substantial oxygen contamination.^{15,16}

B. Germanium deposition

1. Physical vapor deposition (PVD)

After the substrate preparation, the Si wafer was placed immediately into an ion-pumped vacuum system. The vacuum system achieved a baseline pressure of $6\text{--}8 \times 10^{-10}$ Torr after baking. Prior to the Ge deposition, the Si substrate was heated to ~ 500 °C. An increase in fluorine pressure in the vacuum system, monitored by a quadrupole residual gas analyzer, accompanied this heating step indicating the desorption of fluorine from the Si surface. Germanium was then deposited by thermal evaporation from a tungsten boat onto the hot Si surface ($T \sim 500$ °C) at a rate of 3–20 Å/sec. Germanium films 500 Å to 1 μ m thick were obtained in this manner. The system pressure during Ge deposition was $< 10^{-8}$ Torr.

An alternative deposition procedure, which produced amorphous Ge layers (500–2000 Å thick) allowed the Si substrate to cool after the fluorine desorption step. Germanium was then deposited at a rate of > 100 Å/sec onto the cool Si ($T \leq 100$ °C) substrate. These amorphous Ge layers were then crystallized *in situ* by a subsequent heating step ($T \approx 500$ °C for 15 min).

2. Chemical vapor deposition (CVD)

Germanium layers were also deposited on the silicon substrates by the decomposition of germane, GeH₄, using the technique reported in Ref. 6. In this case, the Si substrate after the oxide removal was placed on a graphite susceptor and loaded into a vertical, rf-heated, CVD reactor. The reactor is schematically shown in Fig. 1. The carrier gas in the

reactor at all times consisted of Pd-purified H₂ which had been liquid N₂ cold-trapped prior to introduction into the growth reactor. The Si substrate was heated to the growth temperature which ranged from 500 to 900 °C. This initial heating required 1½ min during which the Si surface was free to react with any residual impurities in the H₂ carrier gas. Germane was then introduced into the reactor to initiate the Ge growth. No intentional dopants were added to the carrier gas. A GeH₄ pressure of 2–13 Torr was used. The Ge growth rate could be varied from 100 to 500 Å/sec by changing the growth temperature and partial pressure of GeH₄.

C. Physical and electrical measurements

The Ge layers obtained above were analyzed by a variety of techniques. The change in surface morphology with the growth parameters of the deposited Ge layers was observed by optical microscopy utilizing Nomarski Interference Contrast. The crystalline perfection of the layers was determined by transmission electron microscopy (TEM), glancing angle x-ray diffraction (Read camera), and 1.5 MeV ⁴He⁺ backscattering spectrometry (BS) and channeling techniques. Both cross-sectional and plan-view transmission electron micrographs were obtained from the CVD and PVD samples under bright field-diffraction contrast for a (220)-type reflection. These micrographs of the Ge layer and Ge-Si interface were used to determine the nature of the crystal defects present in the Ge film.

Electrical characterization of both the Ge film and the resulting Ge/Si heterojunction was also carried out on PVD- and CVD-prepared structures. Mesa-type heterojunction diodes were fabricated by defining circular areas (1 to 2×10^{-4} cm²) using either photolithography or by evaporating Au dots onto the Ge surface through a stainless-steel mask in an ion-pumped vacuum system. The Au dots served not only as an etchant mask in the subsequent etching of the Ge layer (using a modified CP4 etch), but also as an ohmic contact to the Ge. The forward bias current-voltage and the reversed bias capacitance-voltage characteristics were then determined on the resulting diodes. The resistivity and Hall mobility of the layer were found by use of a van der Pauw–Hall technique. All measurements were made at room temperature.

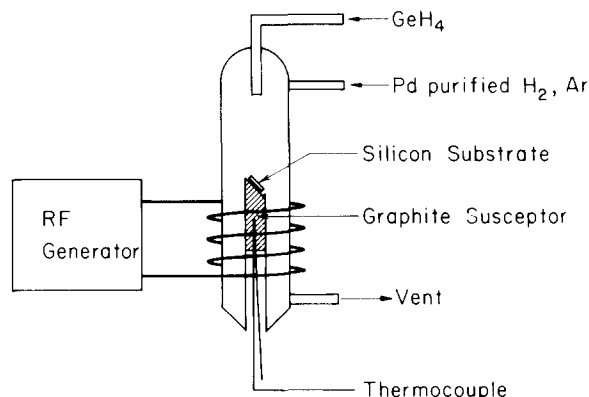


FIG. 1. Schematic diagram of the CVD reactor used in this study. The Pd-purified H₂ used as a carrier gas was liquid N₂ cold-trapped prior to introduction into the reactor.

TABLE I. Properties of PVD grown and CVD grown ($\sim 1 \mu\text{m}$ thick) Ge layers on $\langle 100 \rangle$ Si substrates.

	Physical vapor deposition (PVD)	Chemical vapor deposition (CVD)		
	500 °C	500–600 °C	700–800 °C	900 °C
Surface Morphology (Nomarski Microscopy)	Smooth, specular surface	Smooth, specular surface	Milky, minor surface relief	Rough
Crystalline quality (BS and channeling)	Good epitaxy, surface $\chi_{\min} \approx 4\%–5\%$	Good epitaxy, surface $\chi_{\min} \approx 4\%–5\%$	Poor epitaxy, often polycrystalline	Good epitaxy, surface $\chi_{\min} \approx 4\%–5\%$
Predominant defects (TEM micrographs)	Dislocations	Dislocations	—	Dislocations, stacking faults
Electrical properties (van der Pauw)	$\rho \approx 10^{-2} \Omega \text{ cm}$, p -type, $p \approx 2–4 \times 10^{18} \text{ cm}^{-2}$, $\mu_H = 100–400 \text{ cm}^2/\text{V s}$			

III. RESULTS

The results obtained by the various physical and electrical measurements on both PVD- and CVD-grown Ge are summarized for the case of a $1 \mu\text{m}$ thick Ge layer in Table I.

A. Physical properties of Ge layers

1. Physical vapor deposition (PVD)

Nomarski interference micrographs of Ge layers (500–8000 Å in thickness) deposited onto both the hot ($\leq 500^\circ\text{C}$) and room-temperature (R.T.) Si substrates always showed the Ge layers to be continuous with a smooth surface morphology. Glancing angle x-ray diffraction analyses indicate that a Ge layer deposited onto a hot substrate at low deposition rates ($\leq 20 \text{ Å/sec}$) to be a good quality single-crystal epitaxial layer. The Ge layers deposited onto R.T. substrates with a high deposition rate ($\geq 100 \text{ Å/sec}$) were amorphous in the as-deposited condition. X-ray diffraction patterns taken on these films, after a subsequent *in situ* annealing (500°C , 15 min), indicated the formation of a polycrystalline microstructure in the Ge layer. Amorphous Ge films annealed in a separate vacuum furnace at 750°C for 15 min ($< 10^{-6}$ Torr) gave identical results.

Channeling spectra from Ge layers of varying thicknesses grown on hot substrates at the lower deposition rate are shown in Fig. 2. The crystalline quality at the surface of the Ge layer improves with increasing layer thickness. The channeling minimum yield, χ_{\min} , at the surface of a layer $\geq 4500 \text{ Å}$ in thickness is equal to that of a bulk $\langle 100 \rangle$ Ge crystal having a value of $\chi_{\min} \approx 4\%–5\%$. The subsurface crystalline quality is, however, poorer than bulk $\langle 100 \rangle$ Ge. This can be seen in Fig. 2, where the dechanneling rate in the deposited layers is greater than in bulk $\langle 100 \rangle$ Ge.¹⁷

The TEM micrographs obtained from a sample with an $1 \mu\text{m}$ thick Ge layer are shown in Fig. 3. This sample exhibited good surface crystalline quality as observed in the channeling spectra of this layer ($\chi_{\min} \sim 4\%–5\%$). The cross-section micrograph shows that a misfit dislocation network is generated at the Ge/Si interface to accommodate the lattice mismatch between the two crystals. Dislocations which originate from the network extend into the grown Ge layers.

Layer thicknesses of $> 0.2 \mu\text{m}$ were needed to substantially reduce the density of these dislocations. The corresponding plan view micrograph [Fig. 3(b)] shows a dislocation density of $4 \times 10^9/\text{cm}^2$ near the surface. The oscillating diffraction contrast visible in most of the dislocations indicates that the dislocations are steeply inclined. This is in agreement with the results from the cross-section specimen. Since the plan-view TEM specimen had a wedge-shaped edge, the micrograph was recorded from a thin area ($< 2000 \text{ Å}$ thick) close to the Ge surface. Hence, only the top ends of the dislocations are revealed. The interfacial dislocation network present at a depth of $\sim 1 \mu\text{m}$ is therefore not visible in the plan view micrograph. These misfit dislocations lead to a higher dechanneling yield in the deposited Ge films when compared to bulk $\langle 100 \rangle$ Ge.

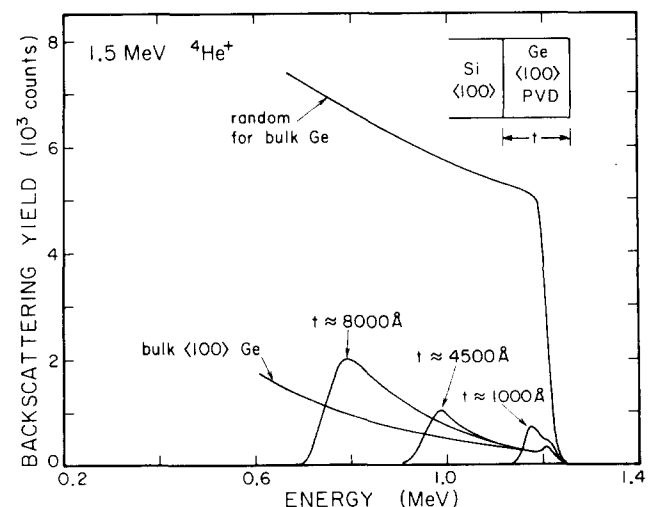


FIG. 2. Channeling spectra taken on PVD-prepared Ge layers grown on heated ($\sim 500^\circ\text{C}$) $\langle 100 \rangle$ Si substrates. A random and an aligned spectrum of a $\langle 100 \rangle$ Ge single crystal are also shown for comparison. The surface minimum yield, determined from the ratio of the aligned spectrum to the random spectrum, decreases with the Ge layer thickness. This indicates the improvement of the crystalline quality at the Ge surface with the Ge layer thickness.

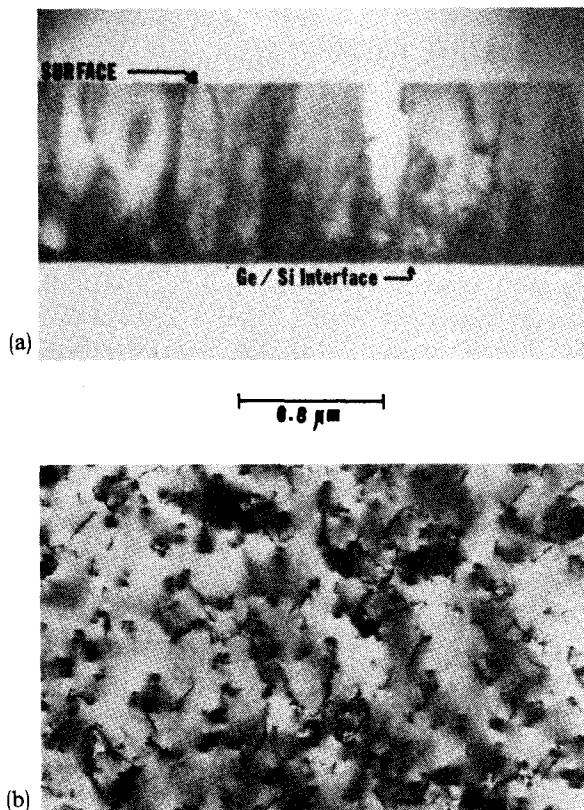


FIG. 3. Cross-sectional (a) and a plan-view (b) transmission electron micrograph taken of a PVD-prepared Ge layer on a <100> Si substrate. The dense dislocation network in the Ge layer, due to the lattice mismatch between Ge and Si is visible both at the Ge-Si interface (a) and at the Ge layer surface (b).

2. Chemical vapor deposition (CVD)

The surface morphology of Ge layers grown by CVD technique on single-crystalline Si substrate has been reported to be a function of the Ge deposition temperature with the surface roughness increasing with increasing temperature.⁶ Increasing the deposition rate at a given temperature, accomplished by raising the GeH_4 partial pressure in the reactor during growth, results in a smoother surface morphology and the formation of a continuous Ge layer at smaller Ge layer thicknesses. The growth rate of the Ge layer could be varied from 100 to 500 Å/sec by altering the temperature and GeH_4 pressure in the growth reactor. At lower growth temperatures (500–700 °C), the Ge growth rate was found to be proportional to the GeH_4 partial pressure for GeH_4 pressures from 2 to 13 Torr. Within this temperature range the Ge growth rate was also exponentially dependent on growth temperature (rate $\propto e^{-Q/k_B T}$). An activation energy Q of approximately $Q \approx 0.49 \pm 0.04$ eV was determined for Ge growth in this temperature range. The growth rate at higher temperatures (800–900 °C) was not as strongly dependent on substrate temperature, but was found to be proportional to the GeH_4 pressure.

Germanium layers grown on Si single-crystal substrates by this CVD technique exhibit varying crystalline perfection depending on deposition temperature (500–900 °C). At low temperatures (500–600 °C), the Ge surface χ_{\min} was found to decrease with increasing layer thickness as

has previously been reported.⁶ A surface χ_{\min} comparable with that of a single-crystal Ge ($\approx 4\%$ – 5%) can be achieved at these temperatures at a layer thickness of ≥ 8000 Å. The subsurface crystalline quality as indicated by the dechanneling rate in the HBS spectra is poorer than that of bulk Ge. Within the intermediate temperature range (700–800 °C), the situation is more complex. The crystalline quality of the Ge layers in this temperature range varies from one deposition to another and is typically poor. Often these layers are found to be polycrystalline. At 900 °C, a continuous Ge film was obtained at a Ge thickness of $\geq 1 \mu\text{m}$ at a deposition rate of 400 Å/sec. Germanium films deposited at 900 °C have always exhibited a good surface crystalline quality ($\chi_{\min} \approx 4\%$ – 5%) although the dechanneling rate is again higher than that found in bulk <100> Ge. Figure 4 shows characteristic channeling spectrum from the three aforementioned temperature ranges for a Ge layer 1.2 μm in thickness.

The TEM micrographs taken of Ge layers deposited at 600 °C indicate a defect structure qualitatively similar to that found on the vacuum deposited layers. The TEM micrographs obtained from Ge layers deposited near 900 °C show, however, a markedly different result as seen in Fig. 5. The cross-sectional TEM micrograph [Fig. 5(a)] revealed the presence of inclined stacking faults and dislocations which nucleate at the Ge/Si interface. A stacking fault density of $\sim 2.2 \times 10^8/\text{cm}^2$ was determined from the corresponding plan view micrograph shown. Some of these stacking faults formed closed rectangular or square figures. The stacking faults always terminated at dislocations that lay along a <110> direction. Occasionally, bundles of stacking faults were also detected in the Ge film. These stacking faults are similar to those observed earlier for epitaxially-grown Si on Si.¹⁸ The higher dechanneling rate found on these layers, when compared to bulk Ge, can again be attributed to this high density of stacking faults and dislocations.

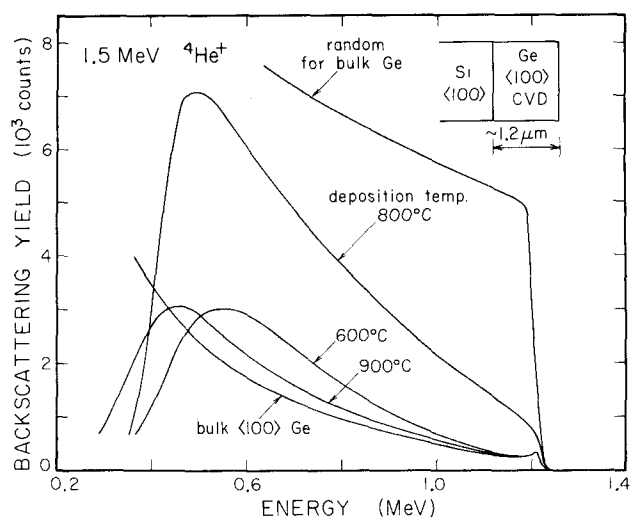


FIG. 4. Channeling spectra taken of CVD-prepared Ge layers grown on <100> Si substrates at different substrate temperatures. The minimum yield at the film surface of the layers grown at 600 and 900 °C is indistinguishable of that of a <100> Ge single crystal. The crystalline quality of a layer grown at 800 °C is poorer.

CVD GROWN Ge LAYER ON <100> Si

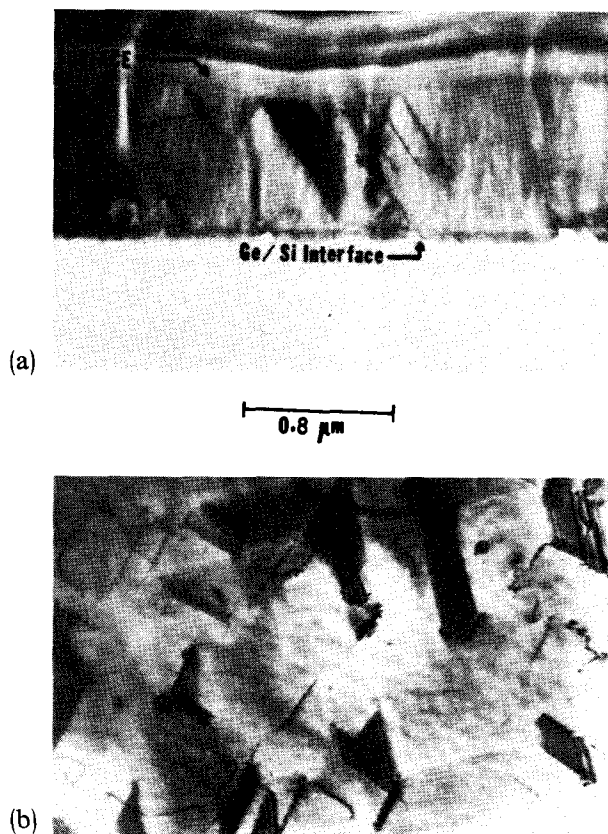


FIG. 5. Cross-sectional (a) and a plan-view (b) micrograph taken on a Ge layer grown by the CVD technique at 900 °C on a <100> Si substrate. The presence of stacking faults and dislocations can be observed in both micrographs.

When considering samples prepared using similar deposition parameters, varying only the temperature, it is seen that the layers grown at 600 and 900 °C possess qualitatively similar channeling spectra. Results obtained from layers grown at intermediate temperatures of 700–800 °C imply poor quality layers are indicative of a partial or complete loss of epitaxy in the Ge film. Contamination of the Si surface prior to Ge growth at 700–800 °C may account for the poor quality of the subsequently grown Ge layer.⁶

In order to investigate the effects of possible contamination of the Si substrate on the resulting Ge layers, silicon substrates were heated in the CVD reactor at 600 °C for varying periods of time before the deposition. Such contamination may result from the residual impurities in the H₂ carrier gas or possibly impurities originating from the graphite susceptor. This waiting period allowed the clean Si surface to react with any such impurities for a controlled period of time. After the waiting period, all substrates received identical depositions yielding Ge layers ~0.5 μm in thickness. These samples were then analyzed by a channeling experiment. The variation in the measured surface χ_{\min} with pre-growth annealing time is given in Fig. 6. If the predeposition annealing time is ≤ 1.5 min, a surface $\chi_{\min} \simeq 6\%$ –7% is typically measured. With longer annealing times, the surface χ_{\min} increases. Waiting times greater than 12 min result in a polycrystalline Ge layer. This result indicates that reactor impurities are most probably responsible for the poor crys-

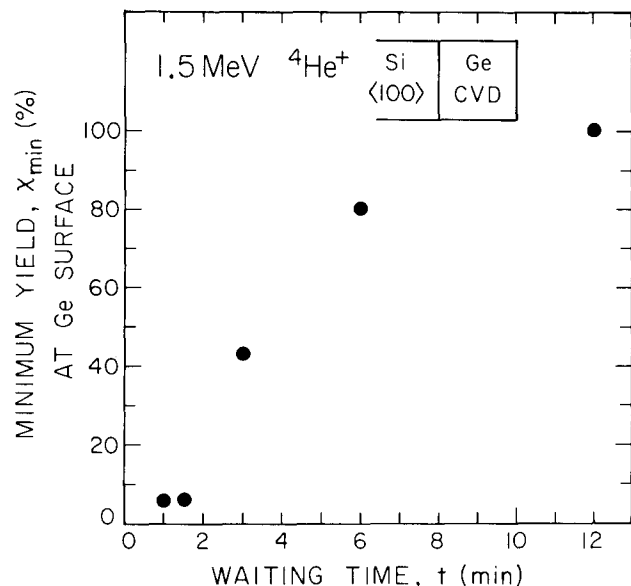


FIG. 6. Minimum yield at the surface of a CVD-prepared Ge layer (~0.5 μm thick) on a <100> Si substrate as a function of the duration of the predeposition substrate heating (waiting time) at 600 °C. The minimum yield increases with the waiting time due to the contamination of the Si substrate prior to the Ge layer deposition.

talline quality and occasional loss of epitaxy within this intermediate temperature range (700–800 °C).

B. Electrical measurements

Room-temperature electrical measurements on PVD-prepared Ge layers deposited on *n*-type Si substrates were carried out using a van der Pauw–Hall technique. The Ge layers are always found to be highly conductive ($\rho \simeq 10^{-2}$ Ω cm, *p*-type) with the hole concentration of $p \simeq 2\text{--}4 \times 10^{18}$ cm⁻³. The average Hall mobility, μ_H , increases with layer thickness from a value of $\mu_H \simeq 100$ cm²/V · s found on thinner layers to that of $\mu_H \simeq 300$ cm²/V · s found with the thicker Ge layers (> 0.8 μm). The hole concentration was constant with layer thickness within the accuracy of this measurement technique. The hole concentrations are, however, well above any impurity level present in the Ge used as a deposition source. The Ge source material had a R.T. resistivity of 0.1 Ω cm (*n*-type).

Similar van der Pauw measurements made on CVD-prepared Ge layers on *n*-type Si substrates indicate that the Ge layers are again highly conductive ($\rho \simeq 10^{-2}$ Ω cm, *p*-type). The hole concentrations and Hall mobilities are comparable to those obtained on the PVD prepared material. A more detailed investigation for the Ge layers deposited at 600 °C shows that the average Hall mobility increases gradually with the Ge layer thickness as shown in Fig. 7. For a layer thickness of ~2000 Å, the Hall mobility is about 100 cm²/Vs. The Hall mobility saturates at a value of ~400 cm²/Vs for layer thicknesses ≥ 8000 Å. The Hall mobility found on the thick Ge layers (≥ 8000 Å) is comparable to that of bulk Ge possessing an acceptor impurity concentration of 10^{18} cm⁻³.¹⁹

Room temperature *I*-*V* and *C*-*V* measurements made in CVD prepared layers are described in detail in Ref. 6. The forward bias *I*-*V* measurements made in that study on the

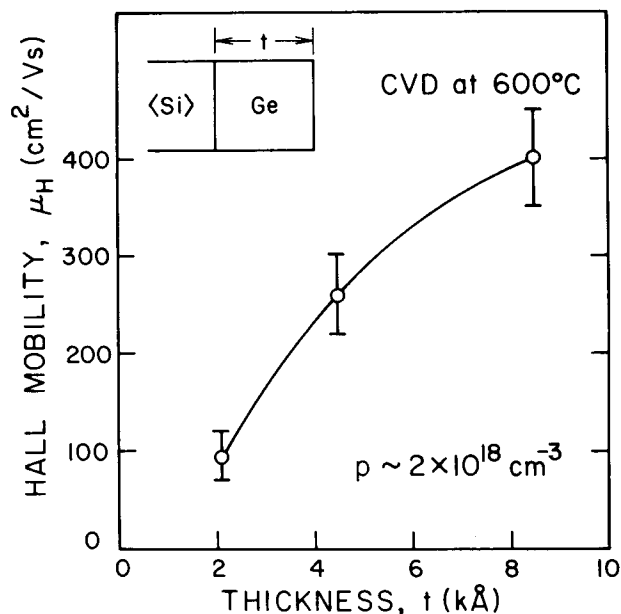


FIG. 7. Hall mobility as a function of Ge film thickness for CVD Ge layers deposited at 600 °C on *n*-type <100> Si substrates. The mobility increases with the layer thickness due to the better average crystalline quality.

p^+ Ge-*n*Si heterojunction diodes were fitted to the equation

$$J = J_0 [e^{qV/nk_B T} - 1], \quad (1)$$

where J is the measured current density, V the applied forward bias, and n is the diode quality factor. A value of $n \leq 1.05$ was obtained from these structures. Reverse-bias capacitance measurements indicate a conductive and valence band discontinuities of $\Delta E_c = 0.05 \pm 0.04$ eV and $\Delta E_v = 0.39 \pm 0.04$ eV, respectively. The results for PVD-grown layers were identical with the limits of measuring error.

IV. DISCUSSION

It is observed that Ge layers grown by PVD and CVD at Si substrate temperatures ≤ 600 °C are qualitatively similar. These layers possess a smooth growth morphology with the surface crystalline quality improving with Ge layer thickness. This is indicated by both the structural and electrical investigations of these films. Physical vapor-deposition films have a slightly better surface crystalline quality and lower dechanneling rate than CVD films at a given layer thickness prepared at 600 °C. Since the initial Si substrate surface is identically prepared in both CVD and PVD growth, the slight improvement found in the PVD may be attributed to the substrate surface contamination found in the CVD layers. This was demonstrated by the pregrowth waiting time experiments discussed above. In both cases, the substantial lattice mismatch between Ge and Si ($\sim 4\%$) is accommodated by the introduction of misfit dislocations as seen in Fig. 4.

The CVD films deposited at high temperatures (~ 900 °C) possess a markedly different defect structure. In these films, a high density of stacking faults are visible in the TEM micrograph of Fig. 5. The appearance of this new microstructure can be due to a variety of causes. The occurrence of these stacking faults appears to be dependent on both the high deposition temperature and the presence of the

Ge-Si interface. The following experiment was conducted in order to verify that these stacking faults originate at the Ge-Si interface and are not induced by a change in Ge on Ge growth mechanism. A PVD Ge layer of 8000 Å thickness was first deposited onto a hot Si substrate (~ 500 °C) in the manner previously described. The sample was then removed from the vacuum system, dipped into a HF : H₂O (1 : 1) etch solution and immediately loaded into the CVD reactor. Another layer of Ge ~ 1.0 μm thick was deposited at ~ 900 °C onto the PVD layer. Identical deposition parameters were used for this Ge layer and the layer shown in Fig. 5. The channeling spectrum of this sample is quantitatively similar to that taken on a CVD Ge layer of similar thickness deposited directly onto the Si surface, exhibiting a $\chi_{\min} = 4\% - 5\%$. There was a striking difference, however, in the results obtained by TEM as shown in Fig. 8. No stacking faults were present in the Ge layer. The sample contained only dislocations at a density $1.8 \times 10^8/\text{cm}^2$. We therefore suggest that the stacking faults nucleate at the Ge-Si interface. The nucleation of stacking faults is probably a result of the formation of a rough Ge/Si interface. This interfacial roughness may arise from two primary causes. The partial coverage of the Si surface by impurities, as mentioned in Sec. III, is a possible source of these stacking faults. Since GeO₂ is easily reduced in the H₂ carrier gas, the subsequent CVD Ge growth on the PVD deposited layer occurs on a clean Ge surface. The clean

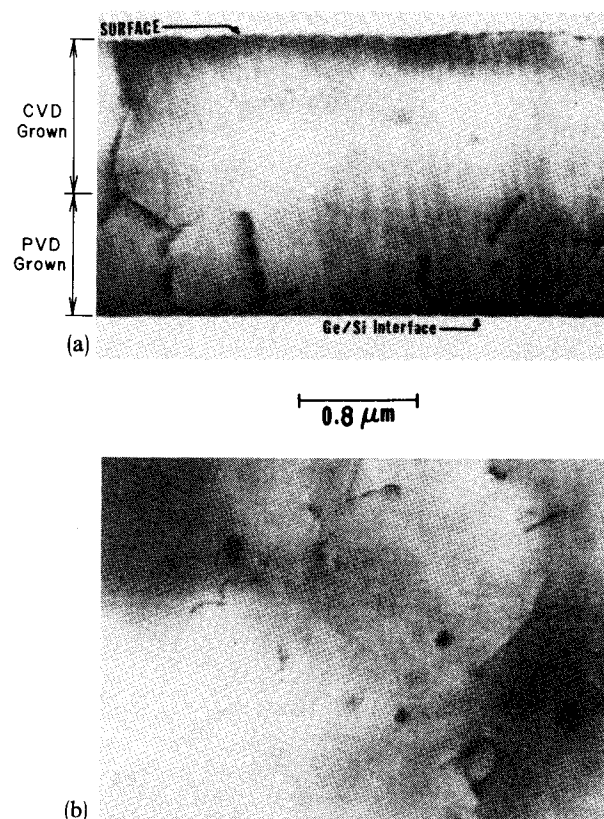


FIG. 8. Cross-sectional (a) and a plan-view (b) transmission electron micrograph taken on a Ge layer grown on <100> Si. Shown in this figure is an initial Ge growth (~ 8000 Å) deposited by the PVD technique with a subsequently deposited CVD layer (~ 1 μm). The main defects are dislocations propagating through the PVD-prepared portion, terminating at PVD Ge-CVD Ge interface.

PVD Ge surface, free of such nucleating centers, yields a subsequent Ge growth devoid of stacking faults. A second source of interfacial roughness in the high-temperature CVD growth may result from the development of a nonuniform layer of Ge-Si solid solution formed at the original Si surface. Additional work using high-resolution TEM and other compositional studies are now under way in order to clarify the nature of this Ge-Si interface.²⁰

It is interesting to observe that the dislocation density at the surface of this CVD Ge layer grown on PVD Ge is much lower than that found in the PVD Ge layer grown on Si at comparable thickness. Examination of the cross-sectional TEM micrograph in Fig. 8 reveals the truncation of several dislocations in the PVD-grown layer at the CVD Ge-PVD Ge interface. The cessation of the Ge on Ge growth and subsequent exposure to air provides a means of decreasing the density of inclined dislocations in any subsequent growth.

Attempts to epitaxially regrow amorphous PVD Ge layers deposited onto room-temperature Si substrate by thermal annealing (750 °C, 15 min), all proved unsuccessful, producing polycrystalline Ge layers. This is in contrast to several earlier studies^{3,5} which used an identical technique to produce epitaxial Ge films. This is surprising since the vacuum deposition environment in this study was at a substantially lower pressure and avoided the carbon impurities associated with the use of an oil-diffusion-pumped system. The absence of nucleation inhibiting impurities in the bulk Ge films, due to the use of an UHV environment, may be a possible cause for the lack of Ge epitaxy.²¹ Structural changes at the clean Si surface subsequent to the heating associated with the fluorine desorption step may also inhibit the nucleation of epitaxial Ge at the interface.²² Further work is needed to verify these hypotheses.

The deposited epitaxial Ge films were found to be highly *p*-type in all cases, such that the hole mobility of these layers increases with layer thickness as does the structural perfection of the Ge layer. These measurements indicate that both the carrier scattering mechanism and probably the source of acceptor type impurity are associated with either point and/or extended crystal defects incorporated into the Ge layer.²³ The *p*-type conductivity of the Ge layer may not be purely associated with the structural defects which result from the Ge-Si lattice mismatch. A previous study of the PVD growth of Ge on Ge substrates, where there is no lattice mismatch, always yielded *p*-type Ge layers.¹² Other acceptors, perhaps point defects or defect complexes unrelated to lattice and thermal mismatch, may therefore determine the conductivity type in deposited Ge films.

Measurements of the conduction and valence band discontinuities in this study ($\Delta E_c = 0.05 \pm 0.04$ eV, $\Delta E_v = 0.39 \pm 0.04$ eV) differ somewhat from that predicted by the method of Anderson based on measured ionization potentials ($\Delta E_v = 0.33$, $\Delta E_c = 0.12$ eV).²⁴ The measured valence-band discontinuity in this study is, however, surprisingly close to the value predicted by the simplified tight binding method developed by Harrison which gives $\Delta E_v = 0.38$ eV.²⁵

Previous determinations of the band discontinuities in

this heterojunction system have shown a large variation in values obtained from junctions fabricated by a particular technique and between junctions formed by varying growth methods.²⁶ The domination of the electrical properties by the electronic and physical structure of the Ge-Si interface is well known, making a definitive determination of the band discontinuities by the present methods difficult.

V. CONCLUSIONS

As observed in this study, both the techniques of vacuum deposition (PVD) and chemical vapor deposition (CVD) have been shown to provide epitaxial Ge layers grown on Si substrates. The crystalline quality of the Ge layers grown by PVD and CVD on Si substrates at temperatures 500–600 °C yield qualitatively similar films. The crystalline quality at the surface of the Ge layer was found to improve with layer thickness. Germanium layers grown by CVD at high temperatures (≈ 900 °C) possessed a markedly different defect structure than the aforementioned films as observed by TEM studies. Electrical studies of both the Ge layer and the resultant Ge-Si interface were presented. These techniques provide a means of providing Ge-coated Si substrates which can be used for the subsequent growth of GaAs or other related compounds.

ACKNOWLEDGMENTS

The authors would like to thank J. O. McCaldin of Caltech for use of equipment and for discussions and encouragement during this study. The authors would also like to thank J. Washburn of the University of California, Berkeley, for useful discussions. The cooperation of the Böhmische Physikalische Society (B. M. Ullrich) is acknowledged. This work was supported in part by the Office of Naval Research (L. R. Cooper) and in part by the U.S. Department of Energy through an agreement with the National Aeronautics and Space Administration and monitored by the Jet Propulsion Laboratory, California Institute of Technology (D. Bickler).

¹S. S. Lau, W. F. Tseng, M.-A. Nicolet, J. W. Mayer, J. Minnucchi, and A. R. Kirkpatrick, *Appl. Phys. Lett.* **33**, 235 (1978).

²H. J. Leamy, C. J. Doherty, K. C. R. Chiu, J. M. Poate, T. T. Sheng, and G. K. Celler, in *Laser and Electron Beam Processing of Materials*, edited by C. W. White and P. S. Peercy (Academic, New York, 1980), p. 581.

³B. Y. Tsaur, J. C. C. Fan, and R. P. Gale, *Appl. Phys. Lett.* **38**, 176 (1981).

⁴B. Y. Tsaur, M. W. Geis, J. C. C. Fan, and R. P. Gale, *Appl. Phys. Lett.* **38**, 779 (1981).

⁵M. Mäenpää, L. S. Hung, M. G. Grimaldi, I. Suni, J. W. Mayer, M.-A. Nicolet, and S. S. Lau, *Thin Solid Films*, **82**, 347 (1981).

⁶T. F. Kuech, M. Mäenpää, and S. S. Lau, *Appl. Phys. Lett.* **39**, 245 (1981).

⁷M. Mäenpää, T. F. Kuech, B. M. Paine, M.-A. Nicolet, D. K. Sadana, and S. S. Lau, Paper presented at the ICVGE-5 and ACCG-5 Conferences, San Diego, California, July 19–24, 1981.

⁸T. F. Kuech, M. Mäenpää, M.-A. Nicolet, D. K. Sadana, and S. S. Lau, Paper presented at the ICVGE-5 and ACCG-5 Conferences, San Diego, California, July 19–24, 1981.

⁹J. C. C. Fan, R. P. Gale, F. M. Davis, and G. Foley, *Appl. Phys. Lett.* **37**, 1024 (1980).

¹⁰M. J. Hampshire and G. T. Wright, *Br. J. Appl. Phys.* **15**, 1331 (1964).

¹¹K. Ito and K. Takahashi, *Jpn. J. Appl. Phys.* **7**, 821 (1968).

¹²G. O. Krause, *Phys. Status Solidi (a)* **3**, 907 (1970).

- ¹³A. G. Cullis and G. R. Booker, *J. Cryst. Growth* **9**, 132 (1971).
- ¹⁴L. N. Aleksandrov, R. N. Lovyagin, O. P. Pchelyakov, and S. I. Stenin, *J. Cryst. Growth* **24/25**, 298 (1974).
- ¹⁵L. S. Hung, S. S. Lau, M. von Allmen, J. W. Mayer, B. M. Ullrich, J. E. Baker, P. Williams, and W. F. Tseng, *Appl. Phys. Lett.* **37**, 909 (1980).
- ¹⁶S. I. Raider, R. Flitsch, and M. J. Palmer, *J. Electrochem. Soc.* **122**, 413 (1975).
- ¹⁷Details of both the Rutherford backscattering and channeling techniques can be found in *Backscattering Spectrometry*, edited by W. K. Chu, J. W. Mayer, and M-A. Nicolet (Academic, New York, 1978).
- ¹⁸H. J. Queisser, R. H. Finch, and J. Washburn, *J. Appl. Phys.* **33**, 1536 (1962).
- ¹⁹S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1967), p. 40.
- ²⁰D. K. Sadana, J. Washburn, M. Mäenpää, T. F. Kuech, and S. S. Lau (unpublished).
- ²¹P. Germain, K. Zellama, S. Squelard, J. C. Bourgoin, and A. Gheorghin, *J. Appl. Phys.* **50**, 6786 (1979).
- ²²D. J. Chadi, *J. Vac. Sci. Technol.* **16**, 1290 (1979), and references contained therein.
- ²³J. W. MacKay and E. E. Klontz, in *Radiation Effects in Semiconductors*, edited by F. L. Vook (Plenum, New York, 1968), p. 175.
- ²⁴A. G. Milnes and D. L. Feucht, *Heterojunctions and Metal-Semiconductor Junctions* (Academic, New York, 1972), Chap. 2.
- ²⁵W. A. Harrison, *Electronic Structure* (W. H. Freeman, San Francisco, 1980), pp. 252–255 and 425–428.
- ²⁶A. G. Milnes and D. L. Feucht, *Heterojunctions and Metal-Semiconductor Junctions* (Academic, New York, 1972), p. 54, see Table 2.1.